

WHAT IS CLAIMED IS:

- 1 1. A method of fabricating a semiconductor device, the method comprising:
2 providing a workpiece;
3 depositing a porous dielectric material over the workpiece;
4 forming a pattern in the porous dielectric material, the pattern comprising sidewalls;
5 depositing a photosensitive material over the porous dielectric material, wherein the
6 photosensitive material forms a barrier region of photosensitive material within the sidewalls of
7 the pattern in the porous dielectric material, over the sidewalls of the pattern in the porous
8 dielectric material, or both within and over the sidewalls of the pattern in the porous dielectric
9 material; and
10 developing the photosensitive material.
- 1 2. The method according to Claim 1, wherein forming the pattern in the porous dielectric
2 material comprises forming a single or dual damascene pattern.
- 1 3. The method according to Claim 1, wherein depositing the porous dielectric material
2 comprises depositing a low dielectric constant material.
- 1 4. The method according to Claim 3, wherein depositing the low dielectric constant material
2 comprises depositing a material having a dielectric constant of 3.0 or less.
- 1 5. The method according to Claim 3, wherein depositing the low dielectric constant material
2 comprises depositing porous methylsilsesquioxane (MSQ), porous inorganic materials, porous
3 CVD materials, porous organic materials, other non-low-k dielectric materials, or combinations
4 thereof.

- 1 6. The method according to Claim 1, wherein depositing the photosensitive material
2 comprises spinning on a material compatible with the porous dielectric material.
- 1 7. The method according to Claim 6, wherein depositing the porous dielectric material
2 comprises depositing porous methylsilsesquioxane (MSQ), a porous inorganic material, a porous
3 CVD material, a porous organic material, or a non-low-k dielectric material, and depositing the
4 photosensitive material comprises depositing a MSQ material, an inorganic material, a CVD
5 material, an organic material, or a non-low-k dielectric material.
- 1 8. The method according to Claim 1, wherein depositing the photosensitive material
2 comprises depositing photosensitive polyimide, a photosensitive organic material, a
3 photosensitive inorganic material, or benzocyclobutane (BCB).
- 1 9. The method according to Claim 1, wherein the porous dielectric material comprises a
2 plurality of pores, wherein the barrier region comprises photosensitive material soaked into the
3 sidewalls of the porous dielectric material pattern by about one or two pores.
- 1 10. The method according to Claim 1, wherein the barrier region comprises photosensitive
2 material soaked into the sidewalls of the porous dielectric material pattern by about 50 Å or less.
- 1 11. The method according to Claim 1, wherein developing the photosensitive material
2 comprises exposing the workpiece to ultraviolet (UV) light.
- 1 12. The method according to Claim 11, wherein exposing the workpiece to light comprises
2 exposing the workpiece to DUV light in 365 nm, 248 nm, or 193 nm wavelengths.

1 13. The method according to Claim 1, further comprising:
2 depositing a liner over the porous dielectric material and barrier region of photosensitive
3 material; and
4 depositing a conductive material over the liner to fill the pattern in the porous dielectric
5 material.

1 14. The method according to Claim 13, wherein depositing the conductive material
2 comprises depositing copper.

1 15. The method according to Claim 1, wherein all of the photosensitive material is removed
2 from the patterned porous dielectric material after developing the photosensitive material.

1 16. The method according to Claim 1, further comprising depositing an etch stop layer over
2 the porous dielectric material, before forming the pattern in the porous dielectric material.

1 17. The method according to Claim 16, wherein the etch stop layer comprises about 100 to
2 1000 Å of a silicon carbon based material, a carbo-nitride material, a spin-on cap material,
3 silicon nitride, silicon oxides, other insulating materials, a metal, or combinations thereof.

1 18. A semiconductor device, comprising:
2 a workpiece;
3 a porous dielectric material disposed over the workpiece, the porous dielectric material
4 comprising a pattern, the pattern comprising sidewalls; and
5 a barrier region of photosensitive material disposed within, over, or within and over the
6 porous dielectric material sidewalls.

1 19. The semiconductor device according to Claim 18, wherein the pattern in the porous
2 dielectric material comprises a single or dual damascene pattern.

1 20. The semiconductor device according to Claim 18, wherein the porous dielectric material
2 comprises a low dielectric constant material.

1 21. The semiconductor device according to Claim 18, wherein the low dielectric constant
2 material comprises a dielectric constant of 3.0 or less.

1 22. The semiconductor device according to Claim 18, wherein the low dielectric constant
2 material comprises porous methylsilsesquioxane (MSQ), porous inorganic materials, porous
3 CVD materials, porous organic materials, other non-low-k dielectric materials, or combinations
4 thereof.

1 23. The semiconductor device according to Claim 18, wherein the photosensitive material
2 comprises a spin-on material compatible with the porous dielectric material.

1 24. The semiconductor device according to Claim 23, wherein the porous dielectric material
2 comprises porous methylsilsesquioxane (MSQ), a porous inorganic material, a porous CVD
3 material, a porous organic material, or a non-low-k dielectric material, and the photosensitive
4 material comprises a MSQ material, an inorganic material, a CVD material, an organic material,
5 or a non-low-k dielectric material.

1 25. The semiconductor device according to Claim 18, wherein the photosensitive material
2 comprises photosensitive polyimide, a photosensitive organic material, a photosensitive
3 inorganic material, or benzocyclobutane (BCB).

1 26. The semiconductor device according to Claim 18, wherein the porous dielectric material
2 comprises a plurality of pores, wherein the barrier region of photosensitive material is disposed
3 within the sidewalls of the porous dielectric material pattern by about one or two pores.

1 27. The semiconductor device according to Claim 18, wherein the barrier region of
2 photosensitive material is disposed within the sidewalls of the porous dielectric material pattern
3 by about 50 Å or less.

1 28. The semiconductor device according to Claim 18, wherein photosensitive material is
2 developable by exposing the workpiece to ultraviolet (UV) light.

1 29. The semiconductor device according to Claim 28, wherein photosensitive material is
2 developable by exposing the workpiece to DUV light in 365 nm, 248 nm, or 193 nm
3 wavelengths.

- 1 30. The semiconductor device according to Claim 18, further comprising:
2 a liner disposed over the porous dielectric material and the photosensitive material
3 disposed within the sidewalls of the porous dielectric material pattern; and
4 a conductive material disposed over the liner, filling the porous dielectric material
5 pattern.
- 1 31. The semiconductor device according to Claim 30, wherein the conductive material
2 comprises copper.
- 1 32. The semiconductor device according to Claim 18, further comprising an etch stop layer
2 disposed over the porous dielectric material.
- 1 33. The semiconductor device according to Claim 32, wherein the etch stop layer comprises
2 about 100 to 1000 Å of a silicon carbon based material, a carbo-nitride material, a spin-on cap
3 material, silicon nitride, silicon oxides, other insulating materials, a metal, or combinations
4 thereof.
- 1 34. The semiconductor device according to Claim 32, wherein the barrier region comprises
2 photosensitive material disposed over the porous dielectric material sidewalls beneath the etch
3 stop layer, and wherein the barrier region comprise substantially vertical sidewalls.